Design of 2-Megapixel, Global Shutter, 120fps, 5µm-Pixel, ROICs for Colloidal Quantum Dots Image Sensors

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***Abstract* —** This paper presents the design of two novel, full HD Readout Integrated Circuits (ROICs) optimized for image sensors employing colloidal Quantum Dots (cQD). Both ROICs share a common architecture while differing primarily in the pixel design: one implements a simple 3T-sense pixel and the other uses a charge-amplifier (CA) based pixel. The two ROIC selection allows optimization of the sensor performance depending on the specific characteristic of the detector material. A full description of the architecture and circuits highlights the versatility of these ROICs.

I. INTRODUCTION

Recent advances [1, 2] in the use of Colloidal Quantum Dots (cQD) for SWIR and X-ray detection have increased the interest in bringing this type of detectors to existing imaging applications that presently use more expensive detector materials or new applications that will be enabled by lower costs. In this paper we present two ROICs tailored for image sensors based on cQD. The ROICs use the same architecture and interface but have pixels optimized for different application requirements.

II. ROIC SENSORS OVERVIEW

The two ROIC sensors have been manufactured with a 180nm CMOS technology. They use the same basic architecture, with the only significant difference being the pixel design, as described in section III. One of the pixels uses a 3T-like sensing node, whereas the other uses a charge-amplifier for sensing.

The top-level block diagram of the sensors is shown in Figure 1. The pixel array is readout in the bottom periphery through column-parallel Programmable Gain Amplifiers (PGAs) and ADCs, followed by an SRAM-based row buffer, data packing and serializer blocks and the sub-LVDS transmitters. The ROIC operation modes and internal timing are fully programmable through an I2C interface. The ROICs include two Phase-Locked Loops (PLL) for the internal generation of the clocks required by the column-parallel ADC and by the subLVDS data transmission. The ROICs have on-chip voltage and current references, LDOs for the generation of some power supplies and a digital-output temperature sensor that is read through the I2C interface.

The specifications of the ROICs are reported in Table 1. They are based on simulation. Some specifications depend on the characteristics of the detector attached to the ROICs pixel's electrodes. The two ROICs have 1920 columns and 1080 rows. In addition, there are 6 dark rows and 16 dark columns which are also readout at each frame. The pixel pitch for both ROICs design is 5 µm. Thus, the focal plane size is 9.6mm x 5.4mm (diagonal of 11 mm). Both pixels can operate in global shutter. There is one ADC per column with selectable bit depth of 8, 10 or 12 bits. The ROIC frame rate is 120fps at full resolution. The sensor supports control of the Region of Interest (ROI) in the Y direction, which increases the output frame rate inversely proportionally to the size of the selected area relative to the full array size. The PGA gain is selectable between 1 and 4, in steps of 1. The sensor has 4 sub-LVDS data outputs, plus a clock reference output. The subLDVS outputs have a maximum data rate of 1.2Gbps but running at 840Mbps is enough to achieve the specified frame rates.

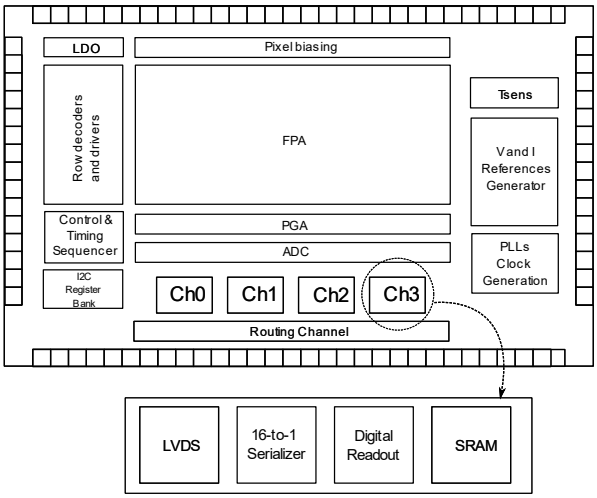

Figure 1. Top-level diagram of sensors.

The screenshot of the die layout of one of the ROICs can be seen in Figure 2 , with all layers shown.

III. PIXELS DESIGN

The schematic of the 3T-sense pixel is shown in Figure 3. The 3T pixel core used for sensing is followed by an in-pixel voltage-mode sampling capacitor for global shutter operation. Node PIXIN is connected to an electrode optimized for CQD. The charge accumulated on this node is sampled on the MOS capacitor MPIXSH when row control signal SAMPLE is driven HIGH. In global-shutter operation, signal sampling is done simultaneously in all pixels of the array. The in-pixel voltage-mode storage requires an in-pixel bias current (see MBIAS and VBIAS) for the 3T-sense source follower (MSF). After the signal voltages are sampled globally, the pixels are read-out in rolling mode through MOUT-MSEL into the Pixel Column. In the default global-shutter mode of the ROICs,

the pixels are reset with global signal GRST to re-start the integration period at the same time on all pixels.

Figure 4 shows the schematic of the CA-based pixel that is used in the other ROIC. In this case the charge collected by the detector diode connected to PIXIN is accumulated on the feedback capacitor C_{ca} and the charge-amplifier (MPAMP-MNAMP) provides a signal voltage output that is sampled onto the in-pixel MOS capacitor (MPIXSH). Like for the 3T-sense pixel, the signal voltage sampling and the pixel reset (through MRST) can be applied globally.

Table 1. Sensor ROICs specifications.

Specification	Value	
Resolution (col. x rows)	1920 x 1080	
Pixel size	5 µm	
Focal plane size	9.6 mm x 5.4 mm	
Focal plane diagonal	11.0 mm	
Die size	13.78 mm x 10.29 mm	
Shutter	Global	
ADC	Column-parallel	
ADC resolution	8, 10 or 12 (user selectable)	
Frame rate (Full HD)	120fps	
Frame rate (ROI: 1980 x 128)	1,010fps	
Programmable Gain (PGA)	1 /2 / 3 / 4	
	ROIC 3T sense	**ROIC CA sense**
Pixel Gain(*)	5.72 µV/e-	14.83µV/e-
Noise (*)	124.5e-rms	90.3e-rms
FW (*)	320ke-	125ke-

(*)*With a detector diode with 25fF capacitance*

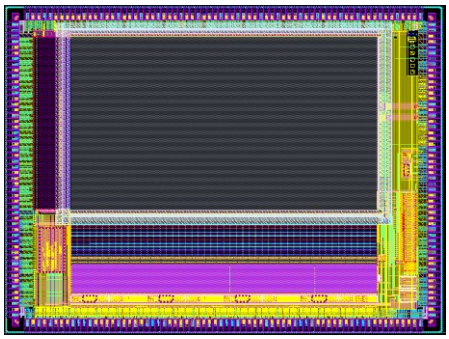

Figure 2. Top-level ROIC layout.

When connected to a detector diode with a capacitance of 25fF, the ROIC with 3T-sense pixel has a gain of 5.72µV/e-, a noise of 124.5e-rms and a FWC of 320ke-. In contrast the ROIC with CA-sense pixel has a gain of 14.83µV/e- and a FWC (125ke-) that are mostly independent of the detector diode capacitance. When a detector diode with 25fF of capacitance is assumed, the noise of the CA-sense pixel is 90.3e-rms. Different applications and cQD detectors will benefit from the gain and FWC specifications of one ROIC or the other, depending on their requirements.

IV. COLUMMN READOUT

The circuits of the pixel column readout are shown in Figure 5. The pixel columns are connected at the bottom periphery to PGAs followed by S&H pairs. The ROIC pixels presented have only one in-pixel voltage storage capacitance. Thus, it is not possible to implement pixel CDS in the PGA in global shutter mode. Instead, when the PGA is reset, it is driven by a PGA reset buffer and its output stored in the first sampling capacitor CSH1. The PGA reset sample will be converted by the ADC. This allows removing PGA kT/C noise and offset with the digital subtraction implemented by the ADC arithmetic block. Following the PGA reset sample, the pixel column signal is read and the output stored in the CSH2 capacitor. The number of parallel MIM capacitors enabled for the input and feedback capacitance of the PGA is adjustable through I2C registers.

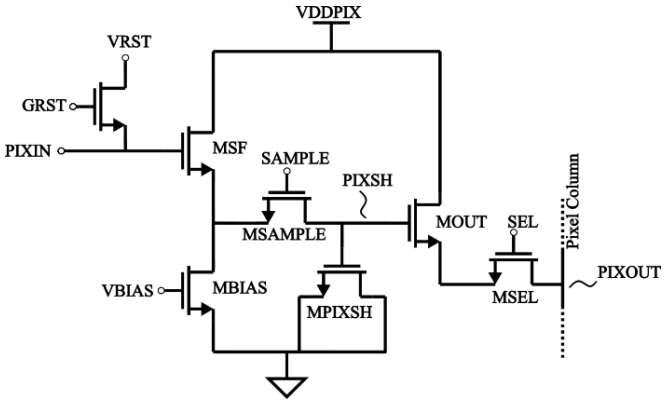

Figure 3. Schematic of 3T-sense pixel.

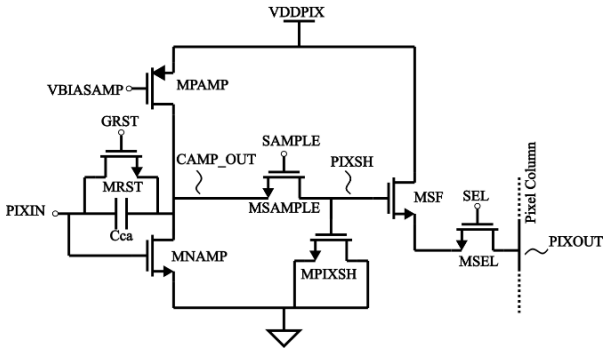

Figure 4. Schematic of charge-amplifier-sense pixel.

In Figure 7 we can see the signal transfer curves at each stage of the readout chain, based on simulation results. The non-linearity is less than 0.1% for the charge amplifier pixel ROIC and less than 0.23% for the 3T-sense pixel. The main reason for this difference is the larger FW (and larger output voltage swing) of the 3T-sense pixel.

The architecture of the 12-bit single-slope ADC that follows the PGA and S&H pair is shown in Figure 6. There is a switched-cap-based ramp generator outside the column-readout array that generates the on-chip MIM-capacitor dependent current from the on-chip bandgap voltage reference. Copies of this current are sent to the column array to create a voltage ramp applied to the ADCs input comparators. The output of a counter driven by an 800MHz clock generated on-chip is distributed along the array to the memory latches. The digital ADC control block synchronizes the counter start, the distributed ramp generator reset and the ADC arithmetic block. Inside the array, the voltages stored in the S&H (PGA reset and pixel signal) are compared with the ramp voltage. The digital code of the counter in the latches keeps the value of the counter output of the moment the ramp reaches the value of the S&H output (see also Figure 9). The ADC arithmetic

unit subtracts the reset digital value from the signal conversion and thus removes any PGA and comparator non-idealities. The ADC output is serialized out to the SRAM blocks.

V. DATA SERIALIZATON AND TIMING

Figure 8 shows the architecture of the block that packs and serializes the output data. The output of the ADC is a 12-bit word that is loaded onto a SRAM bank, 4 ADCs at a time. At the output of the SRAM there is a subtractor block for optional baseline level correction. A small digital block, not pictured, then reads the data sequentially from the SRAM banks 48 bits at a time and packs the data into 16 bits words that are further serialized and sent to the LVDS driver. The digital block also manages the synchronization with the rest of the chip and inserts frame and row headers and filler words when necessary, and word-alignment patterns (WAP) for data synchronization at the host.

The timing diagram given in Figure 9 summarizes the pipeline operation of the readout chain. For each frame, there is a global pixel phase, where the signal is sampled to the in-pixel capacitors, followed by a global reset of the accumulation capacitors. Then, for each row the PGA is reset, the pixel column is read and both voltages are stored in the S&H pair between the PGA and the ADC. The ADC uses a short ramp for the reset conversion and long ramp of the signal conversion.

VI. CONCLUSION

We have presented two ROIC designs optimized for cQD-based image sensors. The 3T-sense pixel offers a FWC and gain determined by the detector diode capacitance, while for the charge-amplifier pixel these parameters are independent of the diode capacitance. For the targeted detector diode a lower FWC, higher gain and lower noise can be achieved with the CA-pixel. Simulation results confirm that both architectures can support high frame rates and low non-linearity, making them suitable for cost-effective SWIR and X-ray imaging applications.

VII. REFERENCES

[1] Konstantatos, G., Wang, Y., Peng, L., Malla, A., Schreier, J., Bi, Y., Black, A., Goossens, S. et al. (2024), *Non-toxic colloidal quantum dots enable shortwave infrared CMOS image sensor*, Nature Photonics. DOI:10.1038/s41566-023-01345-3

[2] C.M. Zhang et al., *A Quantum-dot-based CMOS Image Sensor with Direct X-ray Conversion for Nondestructive Testing*, these proceedings.

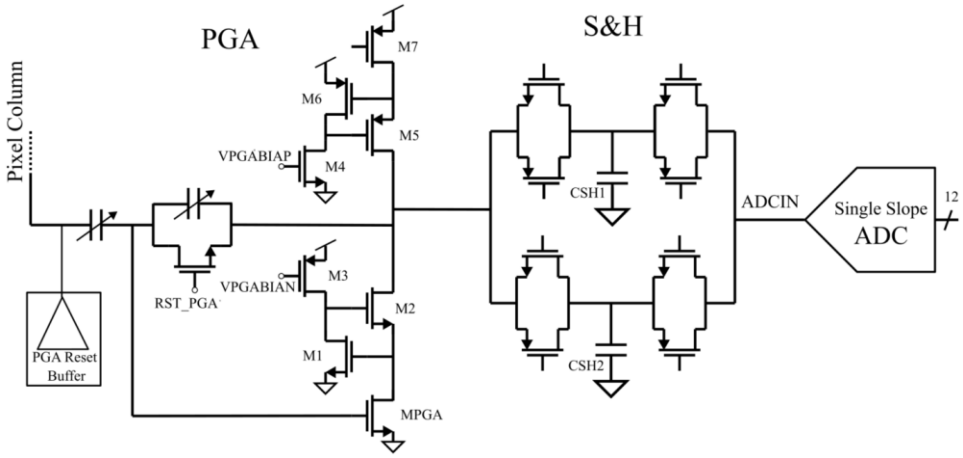

Figure 5. Pixel-column analog readout circuits (PGA and S&H)

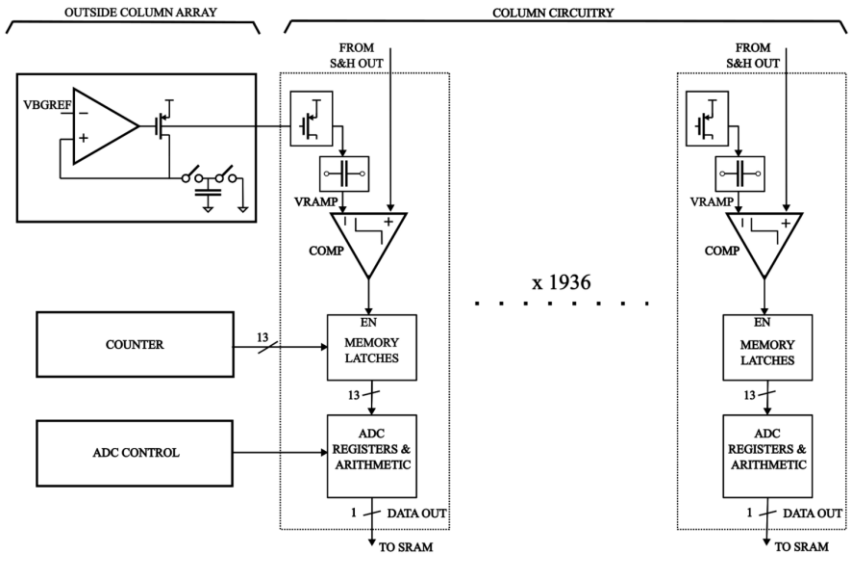

Figure 6. Single-Slope ADC architecture.

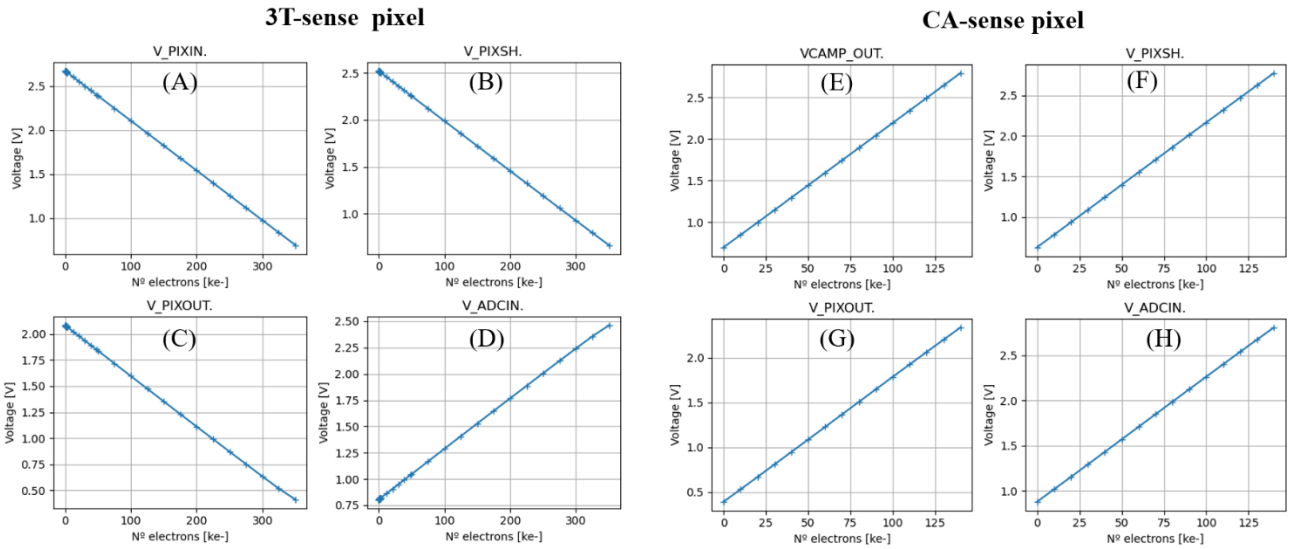

Figure 7. Transfer curves plots through the signal read-out chain. The x-axis is the pixel input signal in ke-. The 4 stages of the R/O chain represented in the plots are: (A) pixel diode node (diode is modeled as a 25fF capacitance); (E) output of the pixel charge amplifier; (B, F) S/H node internal to the pixel; (C, G) pixel column output; (D, H) input to the ADC.

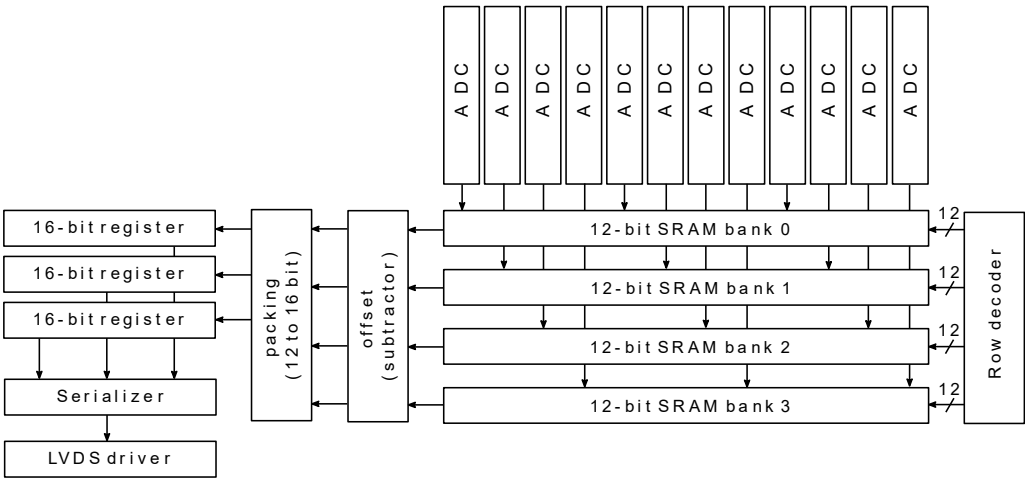

Figure 8. Data serialization and output stream.

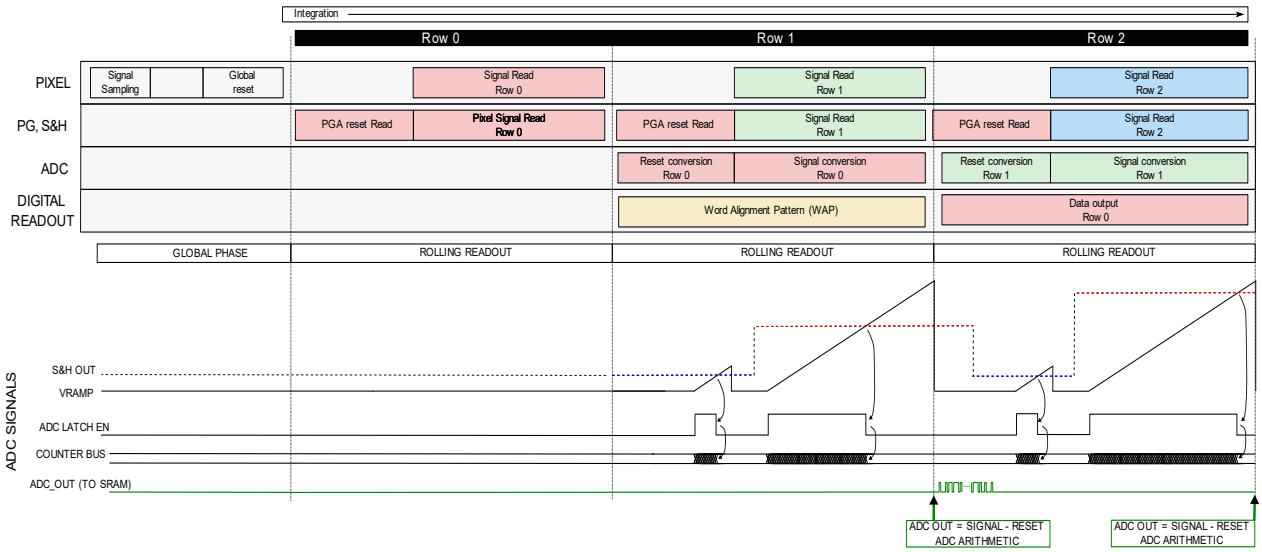

Figure 9. Timing diagram of the ROIC operation.